REMARKS

The Office Action mailed February 15, 2005 has been received and its contents carefully considered.

Claims 11-17 were withdrawn in response to the Election Requirement dated December 20, 2004, and are cancelled herein without prejudice to or disclaimer of the subject matter recited therein. Claim 21 is canceled herein and its limitations incorporated into claim 18. Claims 18-20 are amended herein.

In the current Office Action, the Examiner objects to the title of the invention as not being descriptive. An amended title is proposed herein which is clearly indicative of the invention to which the claims are directed. The Examiner's approval of the amended title is respectfully requested.

The Examiner objects that Figure 4 should be designated by a legend of such as --Prior Art --, on the grounds that only that which is old is illustrated. A Replacement Sheet with Figure 4 revised to include the required legend is attached to the end of this Amendment. The Examiner's approval of the replacement drawing is respectfully requested.

In the Office Action, the Examiner rejects all of the pending claims 18-24 under 35 U.S.C. §102(e) as being anticipated by Ohie, U.S. Patent No. 6,580,164 B1. The claims are amended herein to more clearly distinguish over the applied prior art.

In the method according to amended claim 18, a first semiconductor chip is prepared having a first area that does not generate heat during circuit operation. For example, the first area of the first chip may be formed with a memory that is not used while a second memory on a second semiconductor chip is used instead. The first area on the first chip is larger than the second chip, and the second chip is mounted on the first chip so as to cover an area wholly within the first area of the first chip. Thus, the semiconductor device according to the present invention has the advantage, as described in the application, of reducing the rise in temperature of the stacked semiconductor chips.

With regard to claim 1, the Examiner points to Figures 1-3 of Ohie as disclosing the steps of: preparing the first and second semiconductor chips, the first semiconductor chip (103) having a first area which is free of the formation of elements which generate

heat when in operation, and a second area which surrounds the first area; and mounting the second semiconductor chip on the first semiconductor chip so as to arrange the second semiconductor chip (113) just above the first area of the first semiconductor chip.

The applicant respectfully disagrees. While Ohie does generally disclose a semiconductor device in which a second semiconductor chip is stacked on the first semiconductor chip, there is no teaching or suggestion in Ohie that the area 103a over which the second semiconductor chip is mounted (see Figure 3), is one which is free of the formation of elements which generate heat during operation, as required by claim 18. Rather, the placement of mounting area 103a appears to be determined primarily by the need to facilitate connection of the pad electrodes 125 on the first semiconductor chip to the pad electrodes 115 of the second semiconductor trip chip when the second semiconductor chip is mounted (see, for example, column 6, lines 23-27).

Regarding claim 19, the Examiner points to Figure 5 of Ohie as teaching the method according to claim 18, wherein a microcontroller used as a mask ROM (203) is formed on the first area, and said second semiconductor chip serves a function of a flash memory (213). Figure 5 of Ohie does illustrate an embodiment in which a EEPROM defined as a program memory is formed on an LSI chip 213. An LSI chip 203 having a main surface on which the LSI chip 213 is placed is equipped with a mask ROM defined as a program memory and with all of the circuits required for a micon other than the program memory (see column 10, lines 12-17). However, Ohie fails to disclose that the mask ROM 203 is formed specifically in an area over which the second LSI chip 213 will be mounted, as claim 19 requires. Ohie fails to recognize the benefit in terms of temperature control of mounting the EEPROM, the second chip, over the mask ROM area of the first chip, and so placement of the second chip on the first chip is not considered important. Rather, Ohie focuses on other benefits to be derived from combining the two different chips in a single package, such as reduced manufacturing cost and improved yield (see column 13, lines 3-39).

Regarding claim 21, the limitations of which are now incorporated into claim 18, the Examiner points to Ohie as teaching claim 18, wherein the semiconductor substrate area is larger than the area of the second semiconductor chip. This limitation has been

corrected in amended claim 18 to read " the first semiconductor chip having a first area which is larger than the area of the second semiconductor chip and is free of the formation of elements which generate heat when in operation" (emphasis added). As noted above, Ohie fails to specifically identify "a first area which ... is free of the formation of elements which generate heat when in operation". Thus, although Ohie Figure 5 does disclose that EEPROM 213 is smaller in size than the main LSI chip 203, there is no teaching or suggestion in Ohie that EEPROM 213 is smaller in size than the mask ROM area of the main LSI chip, as claim 21 would require.

It is submitted that for at least the foregoing reasons, claim 18, as well as claims 19-20 and 22-24, as amended, patentably distinguish over the applied prior art reference. Allowance of the application, as amended, is respectfully requested.

Should the Examiner believe that a conference would be helpful in expediting consideration of the application, the Examiner is encouraged to call the undersigned attorney to arrange an interview.

Respectfully submitted,

May 11, 2005
Date

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PGA/rw
Attachment:
Replacement Sheet (Figure 5)

AMENDMENTS TO THE DRAWINGS

Please replace Figure 4 of the drawings with the Replacement Sheet attached to the end of this Amendment.